directed to reduced surface roughness on a conductive surface trace. Thus, the method (i.e., claims 1-6) and the product (i.e., claims 7-18) are related and are not independent from each other. Accordingly, it is respectfully submitted that the election/restriction requirement is improper, and the withdrawal of such election/restriction requirement is respectfully requested.

II. THE ANTICIPATION REJECTION OF CLAIMS 1-6, 19, AND 20

On pages 2-4 of the Office Action, claims 1-6, 19, and 20 were rejected under 35 U.S.C. § 102(b) as being anticipated by Tanaka et al. (U.S. Patent No. 4,959,507). This rejection is hereby respectfully traversed.

Under 35 U.S.C. § 102, the Patent Office bears the burden of presenting at least a prima facie case of anticipation. In re Sun, 31 USPQ2d 1451, 1453 (Fed. Cir. 1993) (unpublished). Anticipation requires that a prior art reference disclose, either expressly or under the principles of inherency, each and every element of the claimed invention. Id.. "In addition, the prior art reference must be enabling." Akzo N.V. v. U.S. International Trade Commission, 808 F.2d 1471, 1479, 1 USPQ2d 1241, 1245 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987). That is, the prior art reference must sufficiently describe the

claimed invention so as to have placed the public in possession of it. In re Donohue, 766 F.2d 531, 533, 226 USPQ 619, 621 (Fed. Cir. 1985). "Such possession is effected if one of ordinary skill in the art could have combined the publication's description of the invention with his own knowledge to make the claimed invention." Id..

Regarding claim 1, the Examiner asserts that Tanaka et al. teaches the claimed invention. Applicants respectfully disagree for several reasons. Specifically, the Examiner implies that Tanaka et al. teaches a method for improving performance of a signal transmitted via a conductive circuit trace of a circuit board as set forth in claim 1. However, as acknowledged by the Examiner, Tanaka et al. teaches a method for forming a bonded ceramic-metal composite substrate. Thus, the teaching of Tanaka et al. clearly differs from the claimed method as set forth in claim 1.

Also, the Examiner asserts that Tanaka et al. teaches reducing a surface roughness of at least one surface of the conductive circuit trace on the surface of the circuit board layer so as to improve performance of a signal transmitted via the conductive circuit trace, as claimed. However, Tanaka et al. fails to teach, or even suggest, improving the performance of a signal transmitted via a conductive circuit trace by

reducing a surface roughness of at least one surface of the conductive circuit trace, as claimed. Indeed, Tanaka et al. fails to teach, or even suggest, anything regarding polishing a copper circuit sheet so as to improve performance of a signal transmitted via the conductive circuit trace, as claimed. Instead, Tanaka et al. teaches polishing a copper circuit sheet so as to improve heat transmissivity between the copper circuit sheet and an electronic component (e.g., see from column 3, line 64, to column 4, line 13). Indeed, Tanaka et al. even teaches that polishing is only required where an electronic component is to be mounted to a copper circuit sheet so as to improve heat transmissivity therebetween, and that polishing is not required where the electronic component is electrically connected to copper circuit sheet, which would be where signals are transmitted (e.g., see from column 1, line 67, to column 2, line 7; column 3, lines 1-8). Such a teaching by Tanaka et al. is not even analogous to the claimed invention. Thus, since the method taught by Tanaka et al. is totally different and non-analogous to the claimed invention, Applicants respectfully submit that Tanaka et al. fails to teach, or even suggest, the claimed invention.

In view of the foregoing, it is respectfully submitted that Tanaka et al. fails to teach, or even suggest, the claimed

invention as set forth in claim 1. Thus, is it further respectfully submitted that claim 1 is allowable over Tanaka et al..

Claims 2-6, 19, and 20 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 2-6, 19, and 20 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination. For example, claim 2 recites reducing the surface roughness by electropolishing the at least one surface, electrochemical polishing the at least one surface, electroplating the at least one surface, or vacuum depositing conductive material on the at least one surface. Tanaka et al. fails to disclose any of these claimed techniques. Also, claims 3-5 recite that the surface roughness of the at least one surface is reduced to no more than 20 microinches root-mean-squared (RMS), 10 microinches root-mean-squared (RMS), or 5 microinches root-mean-squared (RMS). The Examiner asserts that Tanaka et al. teaches such surface roughnesses by disclosing that a surface roughness of no more than 3 μm and no greater than 18 μm. However, 20 microinches translates into .508 μm, 10 microinches translates into .254 μm, and 5

microinches translates into .127 μm. Clearly, the claimed surface roughnesses are below the 3 μm minimum set by Tanaka et al. Accordingly, Tanaka et al. fails to disclose any of these claimed surface roughnesses. Further, claim 6 recites that the at least one surface of the conductive circuit trace includes a surface parallel and proximal to the surface of the circuit board or a surface perpendicular to the surface of the circuit board. Tanaka et al. fails to disclose polishing either of these claimed surfaces.

In view of the foregoing, it is respectfully requested that the aforementioned anticipation rejection of claims 1-6, 19, and 20 be withdrawn.

III. THE ANTICIPATION REJECTION OF CLAIMS 1, 2, 6, AND 19

On pages 4-6 of the Office Action, claims 1, 2, 6, and 19 were rejected under 35 U.S.C. § 102(b) as being anticipated by either Taylor et al. (U.S. Patent No. 6,309,528) or Ozeki et al. (U.S. Patent Application No. 2002/0060090). These rejections are hereby respectfully traversed.

Regarding claim 1, the Examiner asserts that both Taylor et al. and Ozeki et al. teach methods for electroplating on at least one surface of a conductive circuit trace. However, it is respectfully submitted that neither Taylor et al. nor Ozeki et

al. teach providing a layer of a circuit board having a conductive circuit trace on a surface thereof, and reducing a surface roughness of at least one surface of the conductive circuit trace on the surface of the circuit board layer so as to improve performance of a signal transmitted via the conductive circuit trace, as claimed. In contrast, Taylor et al. merely discloses a method of depositing metallic conductors onto the surface of circuit boards, wherein conductive metal is deposited to accommodate both small and large features, while Ozeki et al. merely discloses a method for manufacturing a printed circuit board having a shielded transmission line in order to reduce the effects of external noise. Thus, it is respectfully submitted that neither Taylor et al. nor Ozeki et al. disclose, or even suggest, providing a layer of a circuit board having a conductive circuit trace on a surface thereof, and reducing a surface roughness of at least one surface of the conductive circuit trace on the surface of the circuit board layer so as to improve performance of a signal transmitted via the conductive circuit trace, as claimed. Accordingly, it is respectfully submitted that claim 1 should be allowable.

At this point it should be noted that if the Examiner is going to rely upon the theory that the claimed invention is inherent in either Taylor et al. or Ozeki et al., "the examiner

must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993).

Claims 2, 6, and 19 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 2, 6, and 19 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not disclosed, or even suggested, by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned anticipation rejection of claims 1, 2, 6, and 19 be withdrawn.

IV. THE OBVIOUSNESS REJECTION OF CLAIMS 3-5

On pages 5-8 of the Office Action, claims 3-5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Taylor et

al. (U.S. Patent No. 6,309,528) or Ozeki et al. (U.S. Patent Application No. 2002/0060090) in view of Nagai et al. (U.S. Patent Application No. 2002/0155021) or Taylor et al. (U.S. Patent No. 6,558,231). This rejection is hereby respectfully traversed.

Claims 3-5 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 3-5 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, as discussed above, these claims recite additional features which are not disclosed, or even suggested, by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claims 3-5 be withdrawn.

V. THE OBVIOUSNESS REJECTION OF CLAIM 20

On pages 8 and 10 of the Office Action, claim 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Taylor et al. (U.S. Patent No. 6,309,528) or Ozeki et al. (U.S. Patent Application No. 2002/0060090) in view of Lin et al. (U.S. Patent No. 5,273,938). This rejection is hereby respectfully traversed.

Claim 20 is dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claim 20 should also be allowable at least by virtue of its dependency on independent claim 1. Moreover, claim 20 recites additional features which are not disclosed, or even suggested, by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claim 20 be withdrawn.

VI. CONCLUSION

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-0206, and please credit any excess fees to the same deposit account.

Respectfully submitted,

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APPENDIX A

1 (Previously Presented). A method for improving performance of a signal transmitted via a conductive circuit trace of a circuit board, the method comprising the step of:

providing a layer of the circuit board having the conductive circuit trace on a surface thereof; and

reducing a surface roughness of at least one surface of the conductive circuit trace on the surface of the circuit board layer so as to improve performance of a signal transmitted via the conductive circuit trace.

2 (Previously Presented). The method as in Claim 1, wherein the step of reducing the surface roughness includes one of a group consisting of: electropolishing the at least one surface; chemical polishing the at least one surface; electrochemical polishing the at least one surface; chemical-mechanical polishing the at least one surface; mechanical polishing the at least one surface; electroplating the at least one surface; and vacuum depositing conductive material on the at least one surface.

3 (Original). The method as in Claim 1, wherein the surface roughness of the at least one surface is reduced to no more than

20 microinches root-mean-squared (RMS).

4 (Original). The method as in Claim 1, wherein the surface roughness of the at least one surface is reduced to no more than 10 microinches root-mean-squared (RMS).

5 (Original). The method as in Claim 1, wherein the surface roughness of the at least one surface is reduced to no more than 5 microinches root-mean-squared (RMS).

6 (Original). The method as in Claim 1, wherein the at least one surface of the conductive circuit trace includes one of a group consisting of: a surface parallel and distal to a surface of the circuit board; a surface parallel and proximal to the surface of the circuit board; and a surface perpendicular to the surface of the circuit board.

7 (Original). A circuit board for transmitting at least one signal, the circuit board comprising:

at least one conductive circuit trace for carrying at least one signal, the at least one conductive circuit trace having at least one polished surface.

8 (Original). The circuit board as in Claim 7, wherein the at least one polished surface is polished using one a group consisting of: electropolishing; chemical polishing; electroplating; and vacuum deposition.

9 (Original). The circuit board as in Claim 7, wherein a surface roughness of the at least one polished surface is no more than 20 microinches root-mean-squared (RMS).

10 (Original). The circuit board as in Claim 7, wherein a surface roughness of the at least one polished surface is no more than 10 microinches root-mean-squared (RMS).

11 (Original). The circuit board as in Claim 7, wherein a surface roughness of the at least one polished surface is no more than 5 microinches root-mean-squared (RMS).

12 (Original). The circuit board as in Claim 7, wherein the at least one polished surface of the conductive circuit trace includes one of a group consisting of: a surface parallel and distal to a surface of the circuit board; a surface parallel and proximal to the surface of the circuit board; and a surface perpendicular to the surface of the circuit board.

13 (Original). A conductive circuit trace for carrying a signal, the conductive circuit trace comprising:

conductive material having a plurality of surfaces substantially parallel with a direction of propagation of the signal;

wherein the plurality of surfaces includes at least one polished surface having a reduced surface roughness.

14 (Original). The conductive circuit trace as in Claim 13, wherein the at least one polished surface is polished using one of a group consisting of: electropolishing; chemical polishing; electroplating; and vacuum deposition.

15 (Original). The conductive circuit trace as in Claim 13, wherein the reduced surface roughness of the at least one polished surface is no more than 20 microinches root-mean-squared (RMS).

16 (Original). The conductive circuit trace as in Claim 13, wherein the reduced surface roughness of the at least one polished surface is no more than 10 microinches root-mean-squared (RMS).

17 (Original). The conductive circuit trace as in Claim 13, wherein the reduced surface roughness of the at least one polished surface is no more than 5 microinches root-mean-squared (RMS).

18 (Original). The conductive circuit trace as in Claim 13, wherein the at least one polished surface includes one of a group consisting of: a surface parallel and distal to a surface of the circuit board; a surface parallel and proximal to the surface of the circuit board; and a surface perpendicular to the surface of the circuit board.

19 (Previously Presented). The method as in Claim 1, wherein the conductive circuit trace is formed on the surface of the circuit board layer.

20 (Previously Presented). The method as in Claim 1, wherein the conductive circuit trace is affixed to the surface of the circuit board layer.